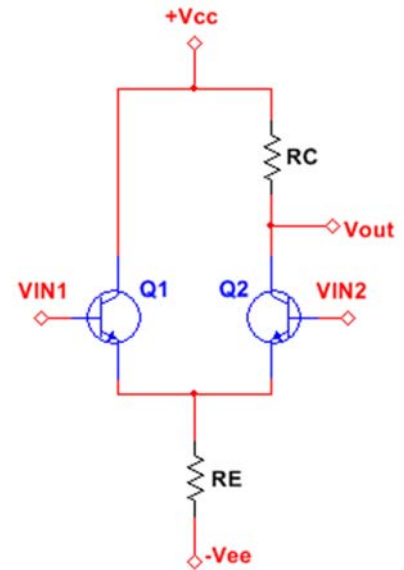


A. Differential Long-Tail Pair

1) Analyze the long-tail pair shown in Fig. 1, where $V_{CC} = +9V$, $-V_{EE} = -9V$, $R_E = 51 \text{ kohm}$ and $R_C = 51 \text{ kohm}$. The inputs are $V_{IN1} = 4V$ and $V_{IN2} = 3.98V$. Assume “quick” analysis parameters ($\beta = 100$, $V_{BE} = 0.7V$, $V_{CE(sat)} = 0V$) for both Q1 and Q2.

- (a) Compute I_{TAIL} and V_{CQ} .
- (b) Compute the differential gain A_d , common mode gain A_{CM} , and CMRR.
- (c) Compute the output $V_{OUT} = V_{CQ} + \Delta V_{OUT}$. Hint: Around 4.5V.
- (d) Compute the input impedance Z_{IN} . Hint: Around 65 kohm.



2) Any amplifier will eventually produce a clipped output signal. This is due to cut-off and/or saturation of a transistor somewhere in the circuit.

Analyze the long-tail pair shown in Fig. 1, where $V_{CC} = +15V$, $-V_{EE} = -15V$, $R_E = 100 \text{ kohm}$ and $R_C = 91 \text{ kohm}$. Suppose $V_{IN1} = 3 + \Delta V/2$ and $V_{IN2} = 3 - \Delta V/2$. Assume “quick” analysis parameters for Q1 and Q2.

- (a) What is V_{CQ} ? Hint: Around 8.6V.
- (b) Compute the differential gain A_d and common mode gain A_{CM} .
- (c) Suppose $\Delta V = 0.02\sin 2\pi f_0 t$, where $f_0 = 2 \text{ kHz}$. Sketch the output $V_{OUT} = V_{CQ} + \Delta V_{OUT}$ over a 1 ms time duration.
- (d) Now make a sketch for $\Delta V = 0.04\sin 2\pi f_0 t$. **Clearly identify the cause of clipped output (Q2 cut-off or saturation).** Hint: Keep in mind that V_{OUT} cannot go higher than V_{CC} !
- (e) Repeat for $\Delta V = 0.06\sin 2\pi f_0 t$. This should cause clipping on both top and bottom portions of the waveform! **Clearly identify the cause of clipping for each portion!**

Fig. 1: Differential long-tail pair for Problems 1 to 3.

3) Design a differential amplifier with $A_d \geq 100$ and $Z_{IN} \geq 50 \text{ k}\Omega$. The power supplies are $V_{CC} = +12V$ and $-V_{EE} = -12 \text{ V}$. Assume Q1 and Q2 have “typical” parameters identical to 2N3904 transistors.

- (a) Compute the necessary tail current I_T .
- (b) Choose the proper value for R_E (standard 5% resistor).
- (c) Based on your choice of R_E , compute your actual I_T and input impedance Z_{IN} .
- (d) Choose the proper value for R_C (standard 5% resistor).
- (e) Based on your chosen values for R_E and R_C , compute the actual gain A_d , quiescent output voltage V_{CQ} , and CMRR of your amplifier.

B. Current Sources

- 4) A voltage source's *current compliance* is the largest load current that can be produced while maintaining the desired output voltage. Similarly, a current source's *voltage compliance* is the largest load voltage that can be produced while maintaining the desired current.

Consider the current source in Fig. 2, where three diodes bias the transistor. Assume each diode produces 0.7V as long as the diode current is roughly 1 mA (+/- 0.2 mA is OK). Assume "quick" analysis parameters for Q1.

- Let $V_{CC} = 9V$. Determine the load current and diode current.
- What is the voltage compliance of this current source? Hint: Think about what causes Q1 to saturate.
- Now suppose V_{CC} drops to 7.5V. Determine the load current, diode current, and voltage compliance.

NOTE: You should find that different V_{CC} has no effect on the load current. This is the advantage of biasing a transistor with a voltage reference (e.g. zener or forward-biased diodes).

- 5) A voltage divider can be used to bias a transistor current source (Fig. 3). Assume "quick" analysis parameters for Q1.

- Is this a stiff voltage divider? Show all work.
- Let $V_{CC} = 9V$. Determine the load current.
- Now suppose V_{CC} drops to 7.5V. Determine the load current.

NOTE: You should find that a drop in V_{CC} affects the load current, which is not good. However, a voltage divider is OK if you know that V_{CC} will be stable (e.g. from a voltage regulator rather than a battery).

- 6) A current source can be operated from split supplies (Fig. 4). Assume +/-9V power supplies, a 5.6V zener, and "quick" analysis parameters for Q1.

- Compute the load current.
- Does the zener have adequate current?
- Compute the voltage compliance of this current source.

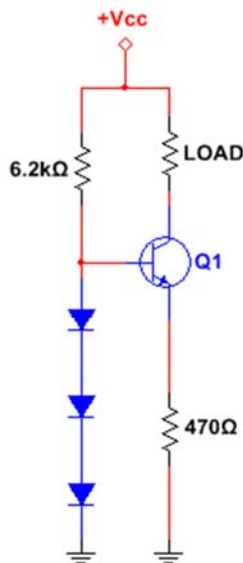


Fig. 2: Problem 4

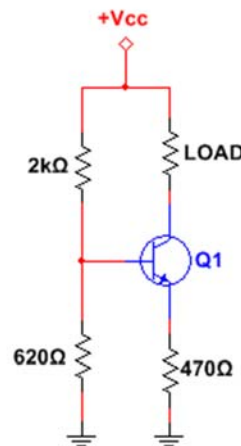


Fig. 3: Problem 5

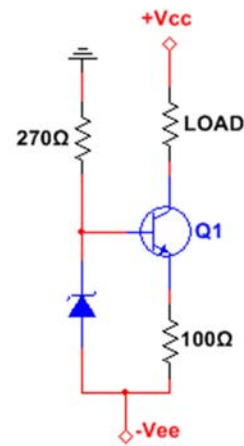


Fig. 4: Problem 6

C. Differential Amplifier Design

- 7) Design a differential amplifier (Fig. 5) with $A_d \geq 120$ and $Z_{IN} \geq 50 \text{ k}\Omega$. The power supplies are $V_{CC} = V_{EE} = 15 \text{ V}$. Assume “typical” 2N3904 parameters for all transistors and “typical” 1N4148 parameters for both diodes.
- Compute the necessary tail current I_T .
 - Choose the appropriate resistors R_1 and R_2 for the current source.
 - Compute the actual I_T based on your choice of components.
 - Choose the proper value for R_C (standard 5% resistor). Hint: Roughly 62 kohm.
 - Compute the actual gain A_d , quiescent output voltage V_{CQ} , and CMRR of your amplifier. Assume the Q3 current source has $R_{OUT} = 5 \text{ Mohm}$. Hint: CMRR is roughly 95 dB.
- 8) Design a differential amplifier with $A_d = 100$ (slightly higher is OK) and $Z_{IN} \geq 10 \text{ k}\Omega$. The power supplies are $V_{CC} = V_{EE} = 12 \text{ V}$. As shown in Fig. 6, five transistors are used. What madness is this? A diode can be made by shorting together the base and collector of a transistor. This technique is commonly used in integrated circuits. Suppose all transistors come from a single LM3046 chip, and assume “typical” LM3046 parameters.
- Compute the necessary tail current I_T .
 - Determine the resistor R_1 , assuming you want about 1 mA of diode current.
 - Use the typical V_{BE} (use appropriate plot and emitter current in data sheet) for Q4 and Q5.
 - Also use the typical h_{FE} for Q3.
 - Determine the resistor R_2 based on your desired I_T .
 - Use the typical V_{BE} (use appropriate plot and emitter current) for Q3.
 - Choose the proper value for R_C (standard 5% resistor), assuming typical h_{FE} . Hint: Roughly 27 kohm.
 - Based on your chosen resistors compute the typical gain A_d and Z_{IN} of your amplifier.

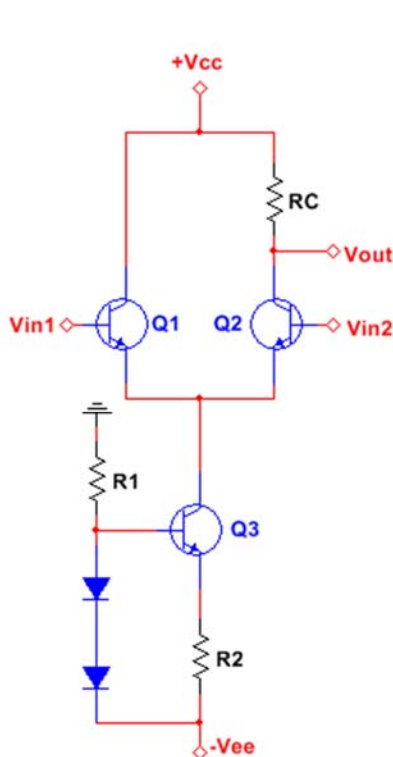


Fig. 5: Problem 7

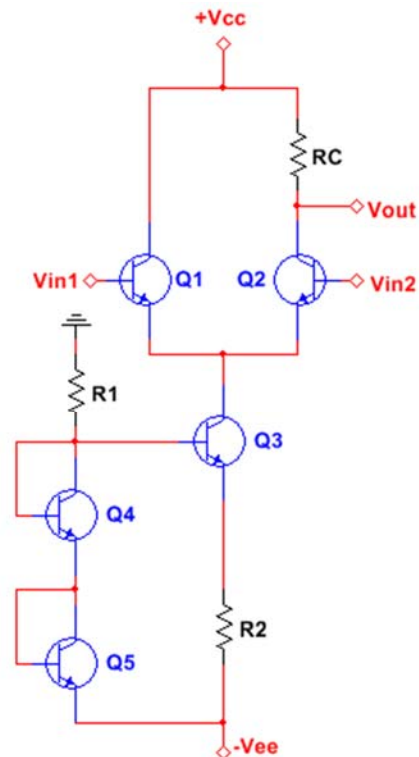


Fig. 6: Problem 8

D. Instrumentation Amplifier

- 9) Weighing scales typically use a load cell to convert weight into a voltage. A load cell is basically a metal beam containing four strain gauges. An applied load causes the beam to bend, producing a differential voltage $\Delta V = V_S \cdot RO \cdot L / L_{RATED}$, where RO is the rated output, L is the applied load and L_{RATED} is the rated load (e.g. maximum recommended load).

This sounds great, but keep in mind that the load cell also produces a common-mode voltage $V_{CM} = V_S/2$. Considering that ΔV is typically 1000 times smaller than V_S , a high CMRR is needed to make sure we can accurately detect tiny load values.

Consider a load cell with $RO = 3 \text{ mV/V}$ and $L_{RATED} = 20 \text{ kg}$. The excitation voltage is $V_S = 10\text{V}$ and the instrumentation amplifier (a special kind of differential amplifier) has a differential gain $A_d = 500$.

- Suppose we live in a fantasy world where $A_{CM} = 0$. What is V_{out} produced by a 20 g load?
- Now we are pulled back to reality, where $A_{CM} \neq 0$. What is the minimum CMRR needed to ensure that the output voltage error from the instrumentation amplifier is less than your answer to part (a)? Hint: Around 104 dB.

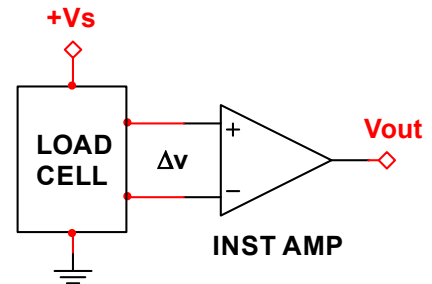


Fig. 7: Load cell amplifier for Problem 9. An “instrumentation amplifier” is a differential amplifier with very high input impedance and CMRR. This makes it compatible with a variety of sensors, even very high impedance ECG electrodes!

- 10) An instrumentation amplifier is a high quality differential amplifier with very high input impedance and CMRR. It is typically made from the 3-op-amp circuit shown in Fig. 8.

- When $V_{IN1} = V_{IN2} = V_{CM}$, use the Golden Rules to show that $V_{OUT1} = V_{OUT2} = V_{CM}$.

Hint: Consider the voltage at each end of R_G using Golden Rule #1, then compute the current through each R_3 , and finally determine the values of V_{OUT1} and V_{OUT2} .

- Show that when V_{IN1} is different from V_{IN2} , then the voltage difference $V_{OUT1} - V_{OUT2}$ is equal to $(1 + 2R_3/R_G) \cdot (V_{IN1} - V_{IN2})$.

Hint: Use a technique similar to solving part (a).

NOTE: A nice feature of this circuit is the gain for $(V_{IN1} - V_{IN2})$ can be much larger than the gain for V_{CM} !

- The third op amp is just a simple differential amplifier with differential gain R_2/R_1 (see HW2, Problem 1). Use the result from Part (b) to show that the instrumentation amplifier’s overall differential gain is $A_d = (1 + 2R_3/R_G) \cdot R_2/R_1$.

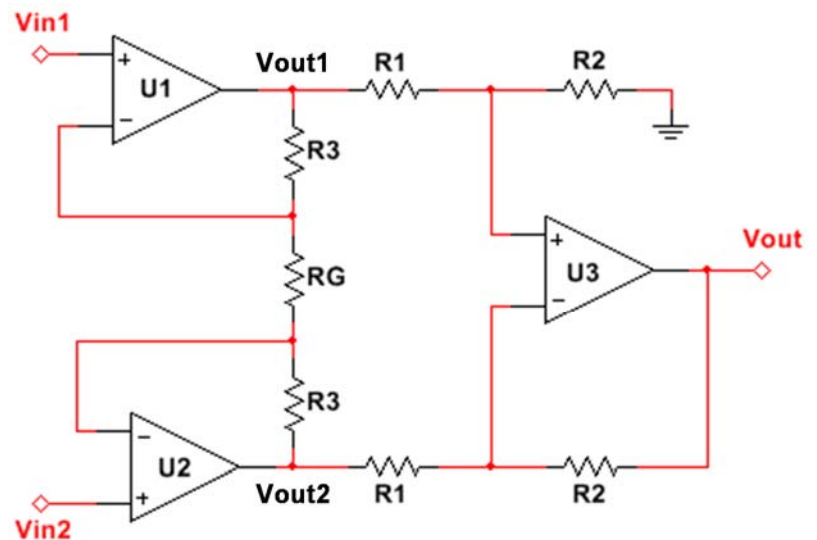


Fig. 8: Three op-amp instrumentation amplifier for Problem 10.