Homework 7
ECE 363 (F19)
8 problems for 100 pts
Due Nov 21

A. Passive Filters

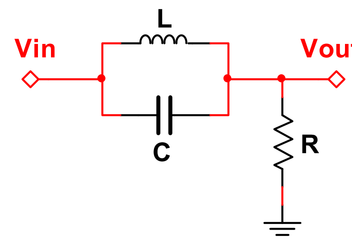


Fig. 1: A "tank circuit" consists of a parallel inductor and capacitor.

1) Consider the "tank circuit" in Fig. 1, where the inductor L and capacitor C are in parallel.

   (a) Sketch the circuit at DC (f = 0) and a separate sketch at really high frequencies ($f \rightarrow \infty$).

   (b) What is V_{OUT}/V_{IN} at these two frequencies?

   (c) Derive an expression for the frequency where the parallel impedance of L and C becomes infinite! This resonant frequency corresponds to energy "sloshing" back and forth between L and C. The trapped energy means nothing gets through, which is the same as infinite impedance.

   (d) Based on your answers to (a) - (c), sketch the magnitude of the frequency response on a linear scale. You do NOT need to calculate anything! Make sure to label your axes. What kind of filter is this?

B. Active Filters

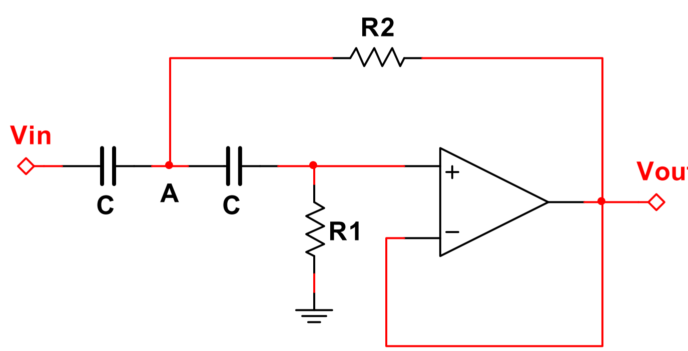


Fig. 2: 2nd order Sallen-and-Key high-pass active filter.

2) Consider the Sallen-and-Key high-pass filter shown in Fig. 2.

   (a) Use the Golden Rules to show that:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-\omega^2 R_1 R_2 C^2}{1 + j2\omega R_2 C - \omega^2 R_1 R_2 C^2}$$

   Hint #1: Since the op amp is basically a buffer, $V_+ = V_- = V_{OUT}$.

   Hint #2: Use KCL at node "A" to obtain V_{OUT} in terms of V_{IN} and V_A.

   Hint #3: What is V_A? V_A and V_+ form a voltage divider, so you can obtain V_A in terms of V_{OUT}.

   (b) Determine expressions for ω_P and Q so that the filter gain from Part (a) has the following form:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-\omega^2/\omega_P^2}{1 + \frac{j\omega}{\omega_P Q} - \omega^2/\omega_P^2}$$

   (c) To make a Butterworth filter, we set Q = 1/sqrt(2) and $f_C = \omega_P/2\pi$. In this case, show that:

$$\left|\frac{V_{OUT}}{V_{IN}}\right| = \frac{\left(\frac{f}{f_C}\right)^2}{\sqrt{1 + \left(\frac{f}{f_C}\right)^4}} \qquad and \qquad f_C = \frac{1}{2\pi\sqrt{R_1 R_2}C}$$

3) Design a 2nd order Butterworth high-pass filter with a "gain" of -50 dB at 500 Hz. Some design constraints:

- Use standard 10% capacitors (see course website). Typical values are between 100 pF and 0.1 uF.
- Use standard 5% resistors. Typical values are between 1 kohm and 1 Mohm.
- If you want, you can combine two resistors in series to make a resistor of twice the value. Or you can combine two resistors in parallel to make a resistor of half the value.

(a) Based on your chosen components, show that your filter gain is within +/-1 dB of the desired value.

(b) **Sketch** the filter gain (in decibels) of your circuit. The frequency axis should be on a log scale from 50 Hz to 500 kHz. For example, your tick marks should show 50 Hz, 500 Hz, 5 kHz, 50 kHz, and 500 kHz. Clearly label your axes and especially the filter gain at 500 Hz, the value of f_C, and the filter gain at f_C.

(c) Sketch your circuit. If you use two resistors in parallel or series, your diagram MUST show this!

4) Higher-order filters produce sharper frequency roll-offs, which is usually a desirable property. They are typically built by cascading lower-order filters. HOWEVER, the lower-order filters are not identical!

Consider a fourth-order Butterworth low-pass filter with f_C = 20 kHz. This requires two second-order filters with f_C = 20 kHz but **DIFFERENT values of Q**! According to Table 19-3 in the textbook, the first stage should have Q = 0.54 while the second stage should have Q = 1.31. Some design constraints:

- Use standard 10% capacitors (see course website). Typical values are between 100 pF and 0.1 uF.
- Use standard 5% resistors. Typical values are between 1 kohm and 1 Mohm.

(a) Design the first stage, and show that its actual f_C (based on your components) is within +/- 5% of 20 kHz.

(b) Repeat for the second stage.

C. Negative Feedback

5) Consider the non-inverting amplifier shown to the right. The op amp has an open-loop gain of $|A_O|$ = 106 dB, differential input resistance R_i = 200 kohm, and output impedance R_O = 25 ohm. Compute the following:

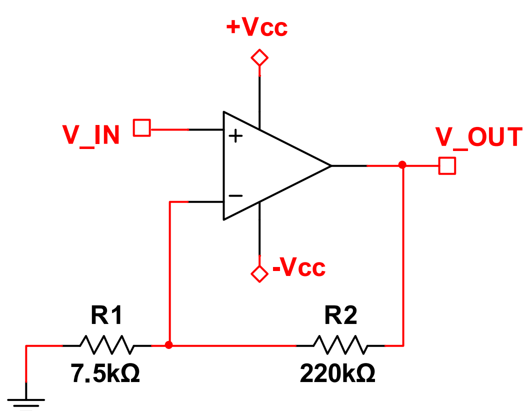
(a) Feedback factor β.

(b) Loop gain $A_O\beta$.

(c) Closed loop gain G.

(d) Input impedance Z_{IN}. Hint: Should be around 1.3 Gohm.

(e) Output impedance Z_{OUT}.



6) You need to design an amplifier with a closed-loop gain of 100 (e.g. 40 dB) that is accurate to within 1% (e.g. $\Delta G/G$ = 1%). You have available some amplifiers with an open-loop gain A_O = 66 dB that are accurate to within +/- 3 dB.

   (a) Based on the nominal gain A_O, what is the necessary β for a single-stage configuration? Remember to compute β to FIVE decimal places (e.g. $\beta = 0.12345$).

   (b) Based on the variation of A_O, what is the closed-loop gain accuracy of this single-stage configuration? Remember to compute G to THREE decimal places (e.g. G = 10.123).

      - Hint: You should get $\Delta G/G$ = 3.5%.

   (c) Assuming two stages with nominal gain A_O, what is the necessary β to produce G = 40 dB?

   (d) Based on the variation of A_O, what is the closed-loop gain accuracy for this double-stage configuration?

      - Hint: You should get $\Delta G/G$ = 0.7%.

7) You are asked to design an amplifier with a gain of G = 30 (not 30 dB) and +/-1% variation (e.g. $G_{MIN} = 29.7$). Due to space requirements on the circuit board, you can only use one stage. Your electronics stockpile has amplifiers with an open-loop gain A_0 that varies by a factor of 10 (e.g. $A_{0,MAX} = 10A_{0,MIN}$) over temperature and time.

   (a) What is the lowest open-loop gain $A_{0,MIN}$ needed for your application?

   Hint #1: $G_{MIN} = 29.7$ is due to $A_{0,MIN}$. Similarly, G_{MAX} is due to $A_{0,MAX} = 10A_{0,MIN}$. Use the expressions for G_{MIN} and G_{MAX} to solve for $A_{0,MIN}$.

   Hint #2: $A_{0,MIN}$ should be around 1350.

   (b) What is the value of β needed for your amplifier? Hint: You should get $\beta = 0.033$.

   (c) What is the nominal gain A_0? Hint: You should get $A_0 = 3000$.

D. <u>Amplifier Stability</u>

8) An amplifier has an open-loop DC gain of A_0 = 10,000 and poles at 1 kHz, 100 kHz, and 10 MHz.

   a) Sketch the Bode plots for magnitude and phase from 1 Hz out to 10 MHz.

   b) Using your Bode plots, find the value of β that produces a phase margin of 45°.

   c) When $\beta = 1$, use your Bode plots to find the frequency where $A\beta = 1$ and compute the resulting phase of A using the exact expression.

   d) Is it OK to make a buffer ($\beta = 1$) with this amplifier?