PreLab 2 – Audio Amplifier

• GOAL

Design an audio amplifier based on an op amp and totem-pole stage.

• OBJECTIVES

Design and simulate the amplifier.

• INTRODUCTION

The overall goal of Lab2 is to demonstrate an audio amplifier. Yes, you could just purchase an IC chip to do this (e.g. LM386), but it is more instructive to build one with an op amp and transistors.

Fig. 1: 16 ohm speaker.

The overall specifications are the following:

- Voltage gain |A| = 6 dB (+/- 0.5 dB is fine) from 400 Hz to 4 kHz
- Input impedance $Z_{IN} \geq 5$ kohm
- Capable of driving a 16 ohm speaker with 75 mW of power.

Some other design constraints are the following:

- Power supply can be V_{CC} = 3, 5, 7, or 9V (choose one).
- The amplifier is non-inverting, which makes it easy to implement volume control with a potentiometer (Fig. 2).
- Use an op amp and Class B totem-pole stage
  - Use an LF356 op amp
  - The npn transistor must either be a 2N3904, 2N4401, or TIP31A.
  - The pnp transistor must either be a 2N3906, 2N4403, or TIP32A.
- Use standard 5% resistors.
  - Keep in mind that R1 is typically between 1 kohm and 10 kohm.
- The signal source and speaker are capacitively coupled to the amplifier (see Fig. 2).
  - You must choose between 1, 4.7, 10, 47, 100, and 470 uF capacitors.
  - At the lowest frequency of interest (400 Hz),
    - The impedance of C_{IN} should have a magnitude that is ten times smaller than Z_{IN}.
    - The impedance of C_{OUT} should have a magnitude that is ten times smaller than R_L.

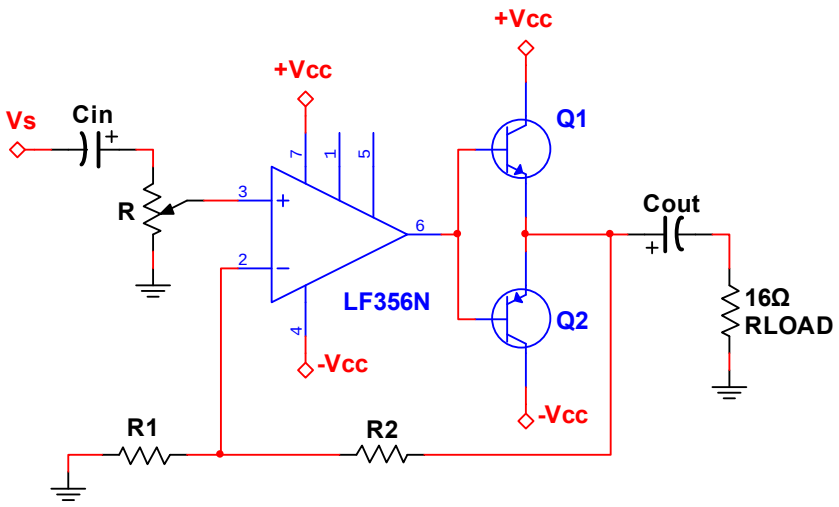

Fig. 2: Non-inverting amplifier op amp with Class B output stage. Volume control is achieved with the potentiometer. At the lowest frequency of interest, the impedances of Cin and Cout should be no more than 1/10 of Zin and R_{LOAD}, respectively.

- **TASK 1**: Compute the maximum peak load voltage and current. Some comments:
  - For now, assume the capacitors act like perfect short circuits (i.e. pretend they are just wires). You will choose their values in TASK 7.
  - Recall that when a resistor R is driven with a sine wave with peak amplitude V_P, the time-averaged power dissipation is $P = V_P^2/(2R)$
  - Hint: You should get around 1.5V and 95 mA.

- **TASK 2**: Choose V_{CC} based on a "quick" analysis ($\beta = 100$, $V_{BE} = 0.7V$, $V_{CE(sat)} = 0V$).
  - Remember to include 2V of headroom!

- **TASK 3**: Choose your npn transistor. Some comments:
  - Technically, power dissipation is NOT constant because both i_C and V_{CE} change with time. **Just to make things easier, let's pretend the peak current and corresponding V_{CE} are constant**.
  - This "quasi DC" approximation overestimates the time-averaged power dissipation. Therefore, a transistor with a power rating that is slightly less than desirable (e.g. $P_{RATING} = 1.5 \cdot P_{MAX}$ instead of $P_{RATING} > 2 \cdot P_{MAX}$) should actually be fine.

- **TASK 4**: Assuming worst-case transistor properties (e.g. min β and max $V_{CE(sat)}$), confirm the LF356 op amp can produce the desired output voltage and current.
  - Remember to use the datasheet tables (not the plots) to find worst-case values!

- **TASK 5:** Would you use a 1 kohm or 10 kohm potentiometer for volume control? Some comments:
  - Assuming Cin is a perfect short, a non-inverting amplifier's input impedance is $Z_{IN} = R$ (see Fig. 2).

- **TASK 6:** Determine the values for R1 and R2. Some comments:
  - The design requirement means the gain can be anywhere between 5.5 and 6.5 dB.

- **TASK 7**: Compute the input and output coupling capacitors C_{IN} and C_{OUT} (show all work). Some comments:
  - We want the capacitor impedance to be negligible at the signal frequencies of interest.
  - The impedance of a capacitor is $Z = 1/(j\omega C)$, so $|Z|$ is largest at the *lowest* frequency of interest f_{MIN}.
  - C_{IN} is in series with the input impedance of the amplifier.
    - Therefore, we want $|Z| < Z_{IN}/10$ at f_{MIN}.
  - Similarly, C_{OUT} is in series with the load resistance R_L.
    - Therefore, we want $|Z| < R_L/10$ at f_{MIN}.
  - Hint: C_{IN} is not that big (e.g. around 1 uF) while C_{OUT} is pretty large (e.g. over 100 uF).

- **TASK 8**: Simulate your circuit using Multisim:
  - We'll use a 16 ohm resistor to approximate the speaker load (this crude model is OK for this lab).
  - V_S comes from an "AC Voltage" source (amplitude = 0.5 Vp and f = 1 kHz).
  - Place two voltage probes: one on the 16 ohm speaker, the other on the op amp output.
  - Run a "transient" simulation for 2 ms submit the plot, and explain the appearance of the op amp output.
  - Measure V_{OUT} at f = 400 Hz, 1 kHz, and 4 kHz.
  - Complete Table 1. Does your voltage gain and max voltage output satisfy the design requirement?

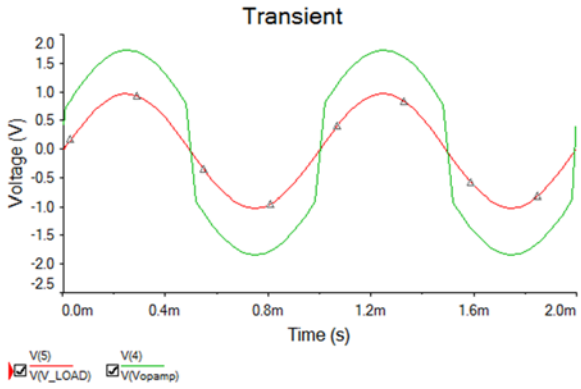

Fig. 3: Your graph at 1 kHz should look something like this.

Table I: Voltage Gain Analysis

f	V_{OUT}	|Gain| (dB)
400 Hz		
1 kHz		
4 kHz		

- **Turn in answers to all tasks, Multisim circuit schematic, and 1 kHz waveform.** (End of PreLab 2)