PreLab 4 – Buck Converter

• GOAL

The goal of Lab 4 is to demonstrate a buck converter to drive a 5V DC brushless fan (e.g. a computer fan).

Fig. 1: 5V DC brushless fan.

• INTRODUCTION

Linear power supplies (e.g. Lab 1) use a pass transistor to act like a "pressure valve" to reduce the +15V input to a stable +5V output. Linear voltage regulators produce a very stable and electrically "clean" output (i.e. no noise spikes). However, they are not very efficient (typically < 30% for a 15V input and 5V output).

Switching power supplies rely on pulse width modulation (PWM) and inductors. They are much more efficient (typically 75% or more). Furthermore, they can produce $V_{OUT} < V_{IN}$ (buck converter), $V_{OUT} > V_{IN}$ (boost converter), and even negative V_{OUT} (buck-boost converter)! The disadvantage is that the rapid switching produces more electrical noise, which can be a problem in applications involving tiny signals. There is always a trade off somewhere!

Fig. 2 is a simplified schematic of a buck converter ($V_{OUT} < V_{IN}$). The inductor acts as a "current storage" element, the diode acts as a voltage clamp for the inductor, while a capacitor smooths the output voltage and current. Q1 is a p-channel power MOSFET, so a logic level shifter Q2 is needed to provide enough gate voltage. A detailed understanding of buck converters is beyond the scope of this course, but this lab will cover some basic concepts.

The design specs fall into two categories.

- For the output: V_{OUT} = 5V, I_{OUT} = 0.22A, $V_{OUT,RIPPLE} < 5\%$.
- For inside the buck converter: $\Delta I/I_{OUT}$= 30% and switching frequency f_{SW} = 50 kHz

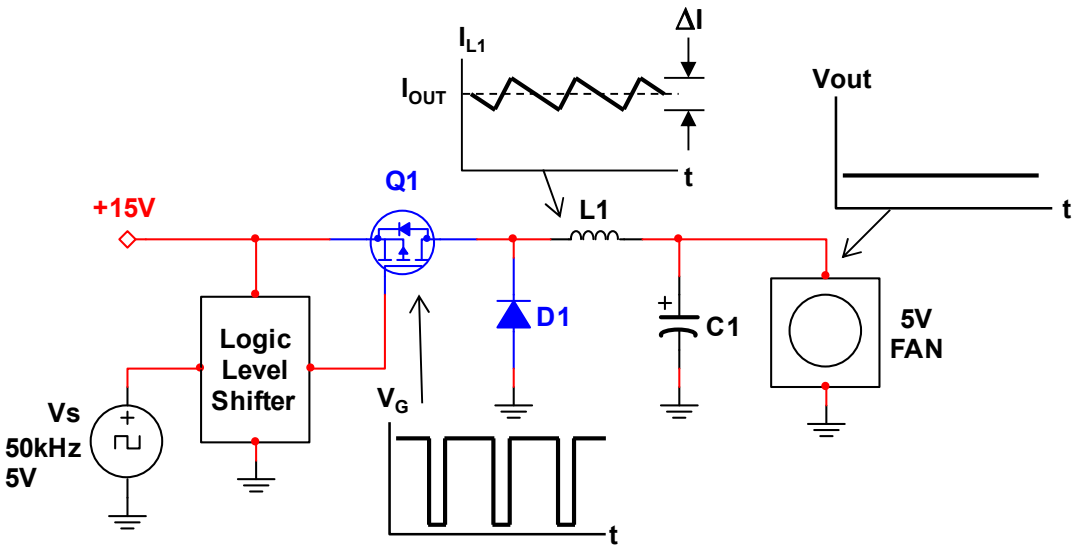

Fig. 2: Simplified schematic of a buck converter. Q1 is the FET switch that is rapidly turned on and off. The inductor current ramps up when Q1 is ON and ramps down while Q1 is off. The capacitor smooths out the voltage and current output.

Some preliminary design calculations are shown below:

- Duty cycle: This is determined by D = Vout/Vin
  - D = 5V / 15V = 0.333.
- Inductor: This is determined by the following formula: $L = V_{OUT} \cdot (1 - D) / (f_{SW} \cdot \Delta I)$
  - $L = 5V \cdot (1 - 0.333) / (50e3\ Hz \cdot 0.3 \cdot 0.22A) = 1.01\ mH \approx 1\ mH$

➢ **TASK 1**: Simulate the buck converter shown in Fig. 3. Some comments:

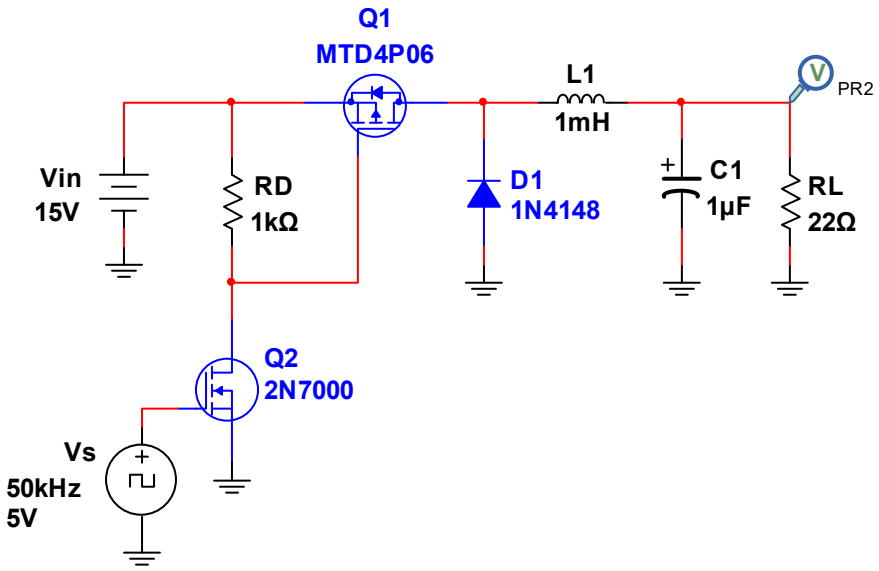

Fig. 3: This is the initial buck converter circuit to simulate in Multisim.

- Q_1: The power switch is an MTD4P06 (p-channel enhancement).
  - This is not exactly what we will use in lab (IRF9520), but it's fine for this prelab assignment.
- Q_2: The logic level shifter is a 2N7000 (n-channel enhancement).
- V_S: The "clock voltage" source is the PWM signal with Freq = 50 kHz, Duty = 33%, Voltage = 5V.
  - Buck converters usually have $f_{SW} > 100$ kHz, but $f_{SW} = 50$ kHz is sufficient for this lab.
- R_D: The 1 kohm drain resistor is chosen for fast switching speed, although power dissipation is pretty high.
- D_1: The 1N4148 diode clamps the inductor voltage while the Q1 switch is off (open).
  - Buck converters usually use Schottky diodes due to their much faster turn on/off speed, but we don't have those in the lab (sorry).
- C_1: The 1 uF filter capacitor is just a starting point.
- R_L: The 22 ohm load is chosen to draw the same current as the 5V fan.
- **Place a voltage probe on V_{OUT} and do a transient simulation with Tstart = 0, Tstop = 2e-4, Tmax = 1e-8.**
  - You should get a waveform that settles to around 6V with some ripple. We want 5V. Interesting ….

- **Move the voltage probe to the Q1 gate voltage and re-run the simulation**.
  - Zoom in on a rising edge. You should see a curved shape (i.e. like charging a capacitor) with a weird little flat spot at around 10V.
  - This flat spot is called the "Miller plateau", which is often a limiting factor in MOSFET switching speed. We'll discuss details later, but two things to keep in mind: (1) the Miller plateau voltage corresponds to the V_{GS} that fully turns on the MOSFET (2) the Q1 gate acts like a big capacitor.
  - ***Turn in this waveform***.
- **Replace R_D with a 10 kohm resistor and re-run the simulation**.
  - The 10 kohm drain resistor results in much less power dissipation, which is good!
  - HOWEVER, you should find that the Q1 gate voltage looks terrible! The rise time is so slow that the gate voltage never reaches 15V! This is very sad.
  - ***Turn in this waveform***.
  - ***Explain why the 10 kohm drain resistor results in such a slow RISE time.***
    - Hint: Think about the circuit path (e.g. a particular resistor) that charges the Q1 gate.
  - ***Explain why the FALLING edge is so much shorter than the rise time.***
    - Hint: Think about the circuit path that discharges the Q1 gate.

➢ **TASK 2**: Modify the logic shifter circuit (Fig. 4) to shorten the rise time of the Q1 gate voltage.

- Keep in mind the following:
  - A capacitor's voltage changes FASTER if the charge/discharge current is LARGER.
  - The logic level shifter can sink (pull) a large current but it can only source (push) a small current.
  - Soooo, we need a push-pull current booster to speed things up!
  - What is an easy way to do this with just two transistors? Hint: Look at HW2, Problem 7.
- Add the push-pull current booster to your logic level shifter (use a 2N3904 and 2N3906).

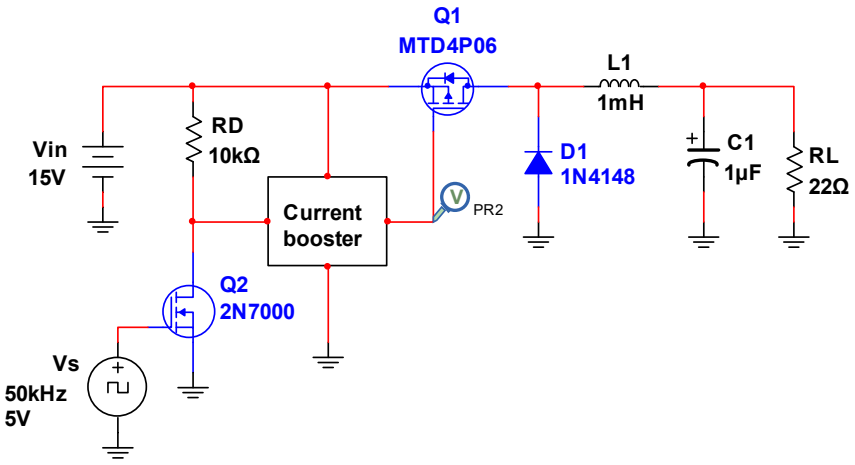

Fig. 4: Add a current booster to more quickly charge/discharge the Q1 gate capacitance!

- Re-run your simulation.
  - You should find a MUCH NICER looking waveform for the Q1 gate voltage!
  - ***Turn in your schematic and the resulting waveform***.
- Move the voltage probe back to monitor V_{OUT} and re-run your simulation.
  - You should find that V_{OUT} is pretty close to 5V (nice!), but not quite. In lab you can tweak the duty cycle to get V_{OUT} to be right on the money.
  - ***Measure the efficiency of your buck converter***.
    - Don't worry about the load voltage not being exactly 5V.
    - You should get a simulated efficiency over 80%. Nice!

➢ **Turn in answers to all tasks, Multisim circuit schematic, and three waveforms.**

(End of PreLab 4)